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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,478	08/22/2003	Daisuke Kawagoe	884.937US1	9311
21186	7590	11/15/2005	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH				PATEL, ISHWARBHAI B
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121 SOUTH EIGHT STREET				PAPER NUMBER
MINNEAPOLIS, MN 55402				2841

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	10/646,478	KAWAGOE, DAISUKE
	Examiner Ishwar (I. B.) Patel	Art Unit 2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 29 September 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 40-58 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 40-58 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 29 September 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

<ol style="list-style-type: none"> 1)<input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2)<input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3)<input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____. 	<ol style="list-style-type: none"> 4)<input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6)<input checked="" type="checkbox"/> Other: <u>Appendix: A, B, C and D</u>.
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DETAILED ACTION

RCE

1. This action is in response to a request for continued examination filed on September 29, 2005.

Drawings

2. The drawings are objected to because the figures are improperly cross-hatched. All of the parts shown in section, and only those parts, must be cross-hatched. The cross-hatching patterns should be selected from those shown on page 600-114/115 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP § 608.02.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 40, ~~41~~⁴² and 44 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumar, US Patent No. 5,227,013.

Regarding claim 40, Kumar, in figure 6, discloses a substrate comprising: a first dielectric layer (41); a second dielectric layer (36); a first conductive layer (42); between the first and second dielectric layers; a third dielectric layer (14); the second dielectric layer being between the first and third dielectric layers; a second conductive layer (34) between the second dielectric layer and the third dielectric layer, the second conductive layer including a first skip via (V1, as marked on figure 6 in appendix "C") that extends

through the first and second dielectric layers; and a third conductive layer (16) on the third dielectric layer, the third conductive layer including a second via (V2, as marked on figure 6 in appendix "C") that extends through the third dielectric layer, the second via and the first skip via being stacked on top of one another (see marked up figure 6).

Regarding claim 41, Kumar further discloses the first skip via includes a longitudinal axis (longitudinal axis passing through the first skip via, V1, see marked up in figure 6, in appendix "C") and the second via includes a longitudinal axis (longitudinal axis passing through the second via, V2, see marked up in figure 6, in appendix "C"), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via (see marked up figure 6, in appendix "C").

Regarding claim 42, Kumar further discloses the first, second and third dielectric layers are formed on a core (base 12, identified in figure 1).

Regarding claim 44, Kumar further discloses the first, second and third conductive layers are patterned conductive layers (see figure 6).

5. Claims 47-49 and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Kumar, US Patent No. 5,227,013.

Regarding claim 47, Kumar, in figure 6F, discloses a substrate comprising: a first dielectric layer (42); a second dielectric layer (36); a first conductive layer

(conductive layer between the dielectric layer 42 and 36) between the first and second dielectric layers; a third dielectric layer (30), the second dielectric layer being between the first and third dielectric layers; a second conductive layer (conductive layer between the dielectric layer 36 and 30) between the second and third dielectric layers, the second conductive layer including a first skip via (V1, as marked on figure 6F in appendix "D") that extends through the first and second dielectric layers; a fourth dielectric layer (14), the third dielectric layer being between the second and fourth dielectric layers; a third conductive layer (conductive layer between the dielectric layers 30 and 40) between the third and fourth dielectric layers; and a fourth conductive layer (conductive layer on dielectric layer 14) on the fourth dielectric layer, the fourth conductive layer including a second skip via (V2, as marked on figure 6F in appendix "D") that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another (see marked up figure 6F).

Regarding claim 48, Kumar further discloses the first skip via and the second skip via each include a longitudinal axis (longitudinal axis of axis of first skip via V1 and second skip via V2), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via (see marked up figure 6F in appendix "D").

Regarding claim 49, Kumar further discloses the first, second, third and fourth dielectric layers are formed on a core (base 12, identified in figure 1).

Regarding claim 51, Kumar further discloses the first, second, third and fourth conductive layers are patterned conductive layers (see figure 6F).

6. Claims 40-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Carpenter et al., US Patent No. 6,810,583 (Carpenter).

Regarding claim 40, Carpenter, in figure 6, discloses a substrate comprising: a first dielectric layer (D1, as marked up on figure 6 in appendix "A"); a second dielectric layer (D2, as marked up on figure 6 in appendix "A"); a first conductive layer (C1, as marked up on figure 6 in appendix "A"); between the first and second dielectric layers; a third dielectric layer (D3, as marked up on figure 6 in appendix "A"); the second dielectric layer being between the first and third dielectric layers; a second conductive layer (C2, as marked up on figure 6 in appendix "A"); between the second dielectric layer and the third dielectric layer, the second conductive layer including a first skip via (57) that extends through the first and second dielectric layers; and a third conductive layer (C3) on the third dielectric layer, the third conductive layer including a second via (26) that extends through the third dielectric layer, the second via and the first skip via being stacked on top of one another (see marked up figure 6 in appendix "A").

Regarding claim 41, Carpenter further discloses the first skip via includes a longitudinal axis (longitudinal axis passing through the first skip via, see marked up in figure 6, in appendix "A") and the second via includes a longitudinal axis (longitudinal axis passing through the second via, see marked up in figure 6, in appendix "A"), the

longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second via (see marked up in figure 6, in appendix "A").

Regarding claim 42, Carpenter further discloses the first, second and third dielectric layers are formed on a core (C5, see marked up in figure 6, in appendix "A").

Regarding claim 43, Carpenter further discloses a fourth conductive layer (C4, see marked up in figure 6, in appendix "A") between the first dielectric layer and the core.

Regarding claim 44, Carpenter further discloses the first, second and third conductive layers are patterned conductive layers (see figure 6).

7. Claims 47-51 are rejected under 35 U.S.C. 102(e) as being anticipated by Carpenter et al., US Patent No. 6,810,583 (Carpenter).

Regarding claim 47, Carpenter, in figure 7, discloses a substrate comprising: a first dielectric layer (D1, marked up on figure 7 in appendix "B"); a second dielectric layer (D2, marked up on figure 7 in appendix "B"); a first conductive layer (C2, marked up on figure 7 in appendix "B") between the first and second dielectric layers; a third dielectric layer (D3, marked up on figure 7 in appendix "B"), the second dielectric layer being between the first and third dielectric layers; a second conductive layer (C3, marked up on figure 7 in appendix "B") between the second and third dielectric layers,

the second conductive layer including a first skip via (V1, marked up on figure 7 in appendix "B") that extends through the first and second dielectric layers; a fourth dielectric layer (D4, marked up on figure 7 in appendix "B"), the third dielectric layer being between the second and fourth dielectric layers; a third conductive layer (C4, marked up on figure 7 in appendix "B") between the third and fourth dielectric layers; and a fourth conductive layer (C5, marked up on figure 7 in appendix "B") on the fourth dielectric layer, the fourth conductive layer including a second skip via (V2, marked up on figure 7 in appendix "B") that extends through the third and fourth dielectric layers, the second skip via and the first skip via being stacked on top of one another (see marked figure 7 in appendix "B").

Regarding claim 48, Carpenter further discloses the first skip via and the second skip via each include a longitudinal axis (longitudinal axis of axis of first skip via and second skip via), the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second skip via (see marked up figure 7 in appendix "B").

Regarding claim 49, Carpenter further discloses the first, second, third and fourth dielectric layers are formed on a core (C7, as marked up on figure 7 in appendix "B").

Regarding claim 50, Carpenter further discloses a fifth conductive layer (C6, marked up on figure 7 in appendix "B") between the first dielectric layer and the core.

Regarding claim 51, Carpenter further discloses the first, second, third and fourth conductive layers are patterned conductive layers (see figure 7).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter, as applied to claim 47 above.

Regarding claim 54, Carpenter discloses all the features of the claimed invention as applied to claim 47 above, including a fifth dielectric layer (D5, marked up on figure 7 in appendix "B"), the fourth conductive layer (C5, marked on figure 7 in appendix "B") being between the fourth and fifth dielectric layers; a sixth dielectric layer (D6, marked up on figure 7 in appendix "B"), the fifth dielectric layer being between the fourth and sixth dielectric layers; a fifth conductive layer (C6, marked up on figure 7 in appendix "B") between the fifth and sixth dielectric layers; a sixth conductive layer (C7, marked up on figure 7 in appendix "B") on the sixth dielectric layer. Carpenter further discloses a third sip via (V3, marked up on figure 7 in appendix "B"), a third skip via that

extends through the fifth and sixth dielectric layers, but does not disclose the sixth conductive layer including connected to the third skip via. However, as can be seen at various places in the figure, the conductor layer / patterns are connected to the via depending upon the desired electrical connection for signal, power or ground connections.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with the third skip via connected to the sixth conductive layer, in order to have desired electric connection for signal, power or ground.

Regarding claim 55, Carpenter further discloses the first, second and third skip vias each include a longitudinal axis, the longitudinal axis of the first skip via being substantially aligned with the longitudinal axis of the second and third skip vias (see marked up figure 7 in appendix "B").

Regarding claim 56, Carpenter further discloses the first, second, third, fourth, fifth and sixth conductive layers are patterned conductive layers (see figure marked up figure 7 in appendix "B").

10. Claims 45-46, 52-53 and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter, as applied to claims 40, 47 and 54 above, and further in

view of Uchikawa et al. US Patent No. 6,531,661 (Uchikawa) and Asai et al., US Patent No. 6,534,723 (Asai).

Regarding claim 45, Carpenter discloses all the features of the claimed invention as applied to claim 40 above, including the first skip via and second via, but does not disclose the first skip via has a diameter between 49 μm and 85 μm and the second via has a diameter between 49 μm and 85 μm . However, the size of the via will depend upon various factor such as the method of making the via, the thickness of the dielectric material and in particular the required current carrying capacity for minimum loss through the via.

Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64).

Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm , to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with the first skip via having a diameter between 49 μm and 85 μm and the second via having a diameter between 49 μm and 85 μm , as taught by Uchikawa and Asai, in order to have desired current carrying capacity.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involve only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 46, Carpenter discloses all the features of the claimed invention as applied to claim 40 above, including the first skip via and the second via, but does not disclose the first skip via has a length between 58 μm and 92 μm and the second via has a length between 24 μm and 36 μm . However, the length of via will depend upon the thickness of the insulating layers of the circuit board and number of insulating board layers the via travels.

As applied to claim 45 above, Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64). Also, Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm , to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with via lengths of both the vias as claimed, as taught by Asai and Uchikawa, in order to have electrical connection between the different layers of the circuit board for transmitting signals.

Regarding claim 52, Carpenter discloses all the features of the claimed invention as applied to claim 47 above, including the first skip via and the second skip via, but does not disclose the first skip via has a diameter between 49 μm and 85 μm and the second skip via has a diameter between 49 μm and 85 μm . However, the size of the via will depend upon various factors such as the method of making the via, the thickness of the dielectric material and in particular the required current carrying capacity for minimum loss through the via.

Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64).

Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm , to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with the first skip via having a diameter between 49 μm and 85 μm and the second skip via having a diameter between 49 μm and 85 μm , as taught by Uchikawa and Asai, in order to have desired current carrying capacity.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involve only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 53, Carpenter discloses all the features of the claimed invention as applied to claim 47 above, including the first skip via and the second skip via, but does not disclose both skip via has a length between 58 μm and 92 μm . However, the length of via will depend upon the thickness of the insulating layers of the circuit board and number of insulating board layers the via travels.

As applied to claim 52 above, Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64). Also, Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm , to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with via lengths of both the vias as claimed, as taught by Asai and Uchikawa, in order to have electrical connection between the different layers of the circuit board for transmitting signals.

Regarding claim 57, Carpenter discloses all the features of the claimed invention as applied to claim 54 above, including the first skip via and the second skip via and the third skip via but does not disclose each via has a diameter between 49 μm and 85 μm . However, the size of the via will depend upon various factor such as the method of making the via, the thickness of the dielectric material and in particular the required current carrying capacity for minimum loss through the via.

Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64).

Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm , to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with each skip via having a diameter between 49 μm and 85 μm , as taught by Uchikawa and Asai, in order to have desired current carrying capacity.

Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involve only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 58, Carpenter discloses all the features of the claimed invention as applied to claim 54 above, including the first skip via, the second skip via and the third skip via but does not disclose the skip vias have a length between 58 μm and 92 μm . However, the length of via will depend upon the thickness of the insulating layers of the circuit board and number of insulating board layers the via travels.

As applied to claim 52 above, Uchikawa discloses printed circuit board with via diameter of 30 to 200 μm and a depth of 0.05 to 0.5 mm (column 4, line 60-64). Also, Asai discloses a circuit board with the insulative substrate with about 20 to 600 μm to

assure a sufficient insulation performance with the diameter of holes within a range of 50 to 200 μm , to facilitate filling of conductive material to have reliable electrical connection (column 11, line 66 to column 12, line 18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter with via lengths of all the skip vias as claimed, as taught by Asai and Uchikawa, in order to have electrical connection between the different layers of the circuit board for transmitting signals.

Response to Arguments

11. Applicant's arguments with respect to claims 40-58 have been considered but are moot in view of the new ground(s) / new explanation of rejection.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Schmidt et al. US Patent No. 6,486,394, in figure 5, discloses skipped via 32 through two dielectric layers 35 and 15, stacked upon a via 22 through a third dielectric layer 25.

Burgess, US Patent No. 6,631,558, in figure 26, discloses skip vias and vias stacked upon each other.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
November 11, 2005

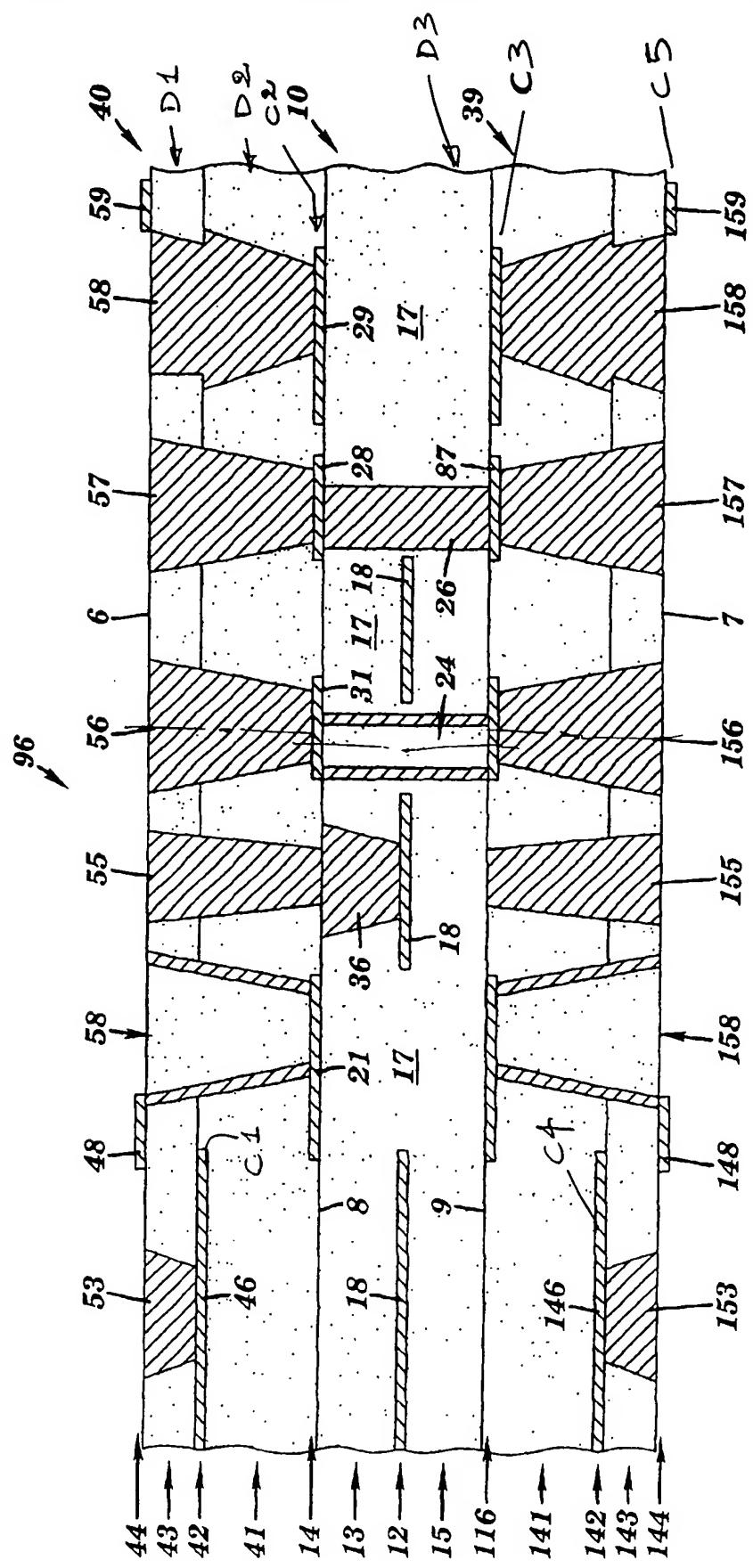


FIG. 6

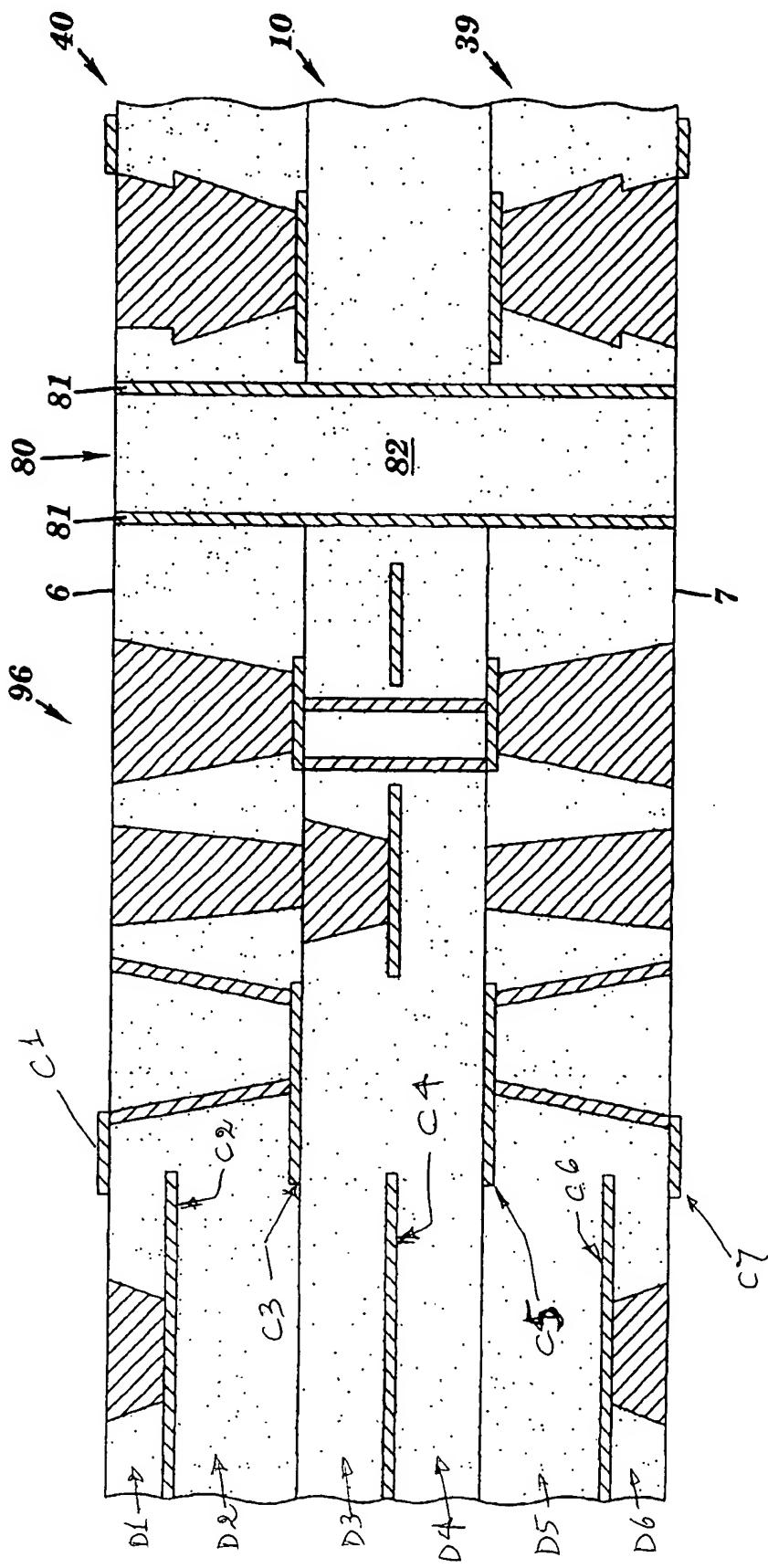


FIG. 7

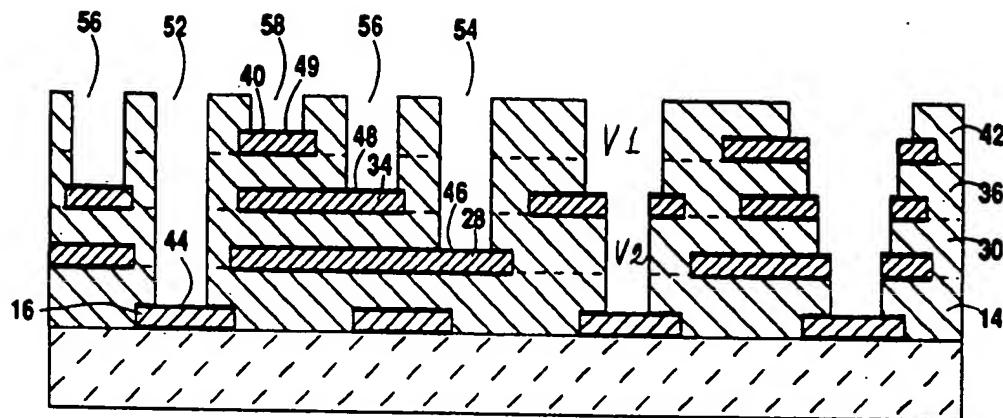


Fig. 6

1 B Balut

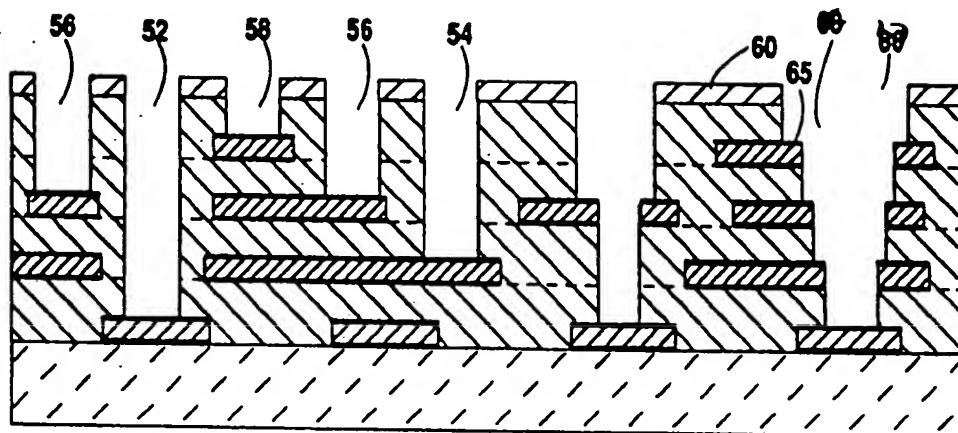


Fig. 6E

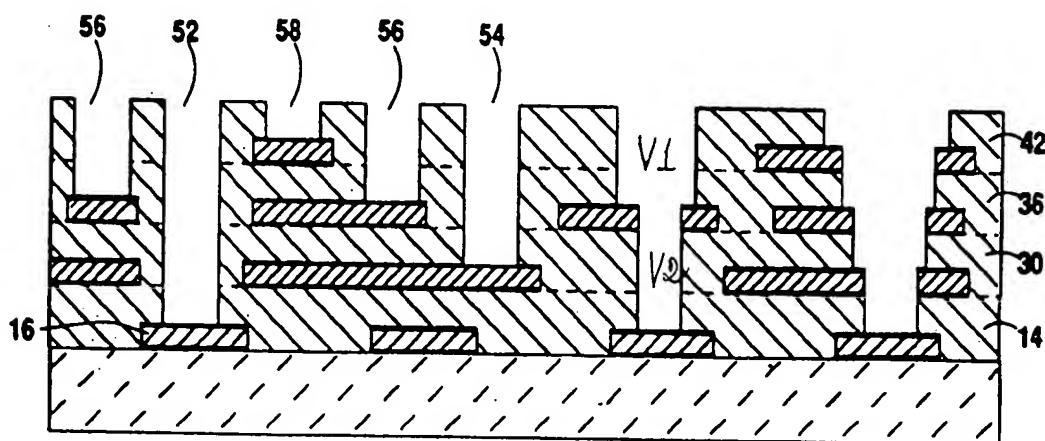


Fig. 6F

IB Parhi